Texas Instruments

# DAC7741EVM

## User’s Guide

October 2002

DAP EVMs

SLAU093

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±15 V and the output voltage range of ±10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than xxx°C. The EVM is designed to operate properly with certain components above xxx°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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## Preface

# Read This First

### *About This Manual*

This user's guide describes the characteristics, operation, and the use of the DA7741 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram and circuit descriptions are included.

### *How to Use This Manual*

This document contains the following chapters:

- ❑ Chapter 1—EVM Overview
- ❑ Chapter 2—Physical Description
- ❑ Chapter 3—EVM Operation

### *Information About Cautions and Warnings*

This book may contain cautions and warnings.

> CAUTION
>
> **This is an example of a caution statement.**
>
> **A caution statement describes a situation that could potentially damage your software or equipment.**

> WARNING
>
> **This is an example of a warning statement.**
>
> **A warning statement describes a situation that could potentially cause harm to you.**

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| **Data Sheets:** | **Literature Number:** |
|---|---|
| DAC7741 | SBAS248 |
| REF102 | PDS-900E |
| OPA627 | PDS-998H |

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## Chapter 1

# EVM Overview

This chapter gives a general overview of the DAC7741 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

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## 1.1 Features

This EVM features the DAC7741 digital-to-analog converter. The DAC7741 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality of the high resolution, single-channel, and parallel input DAC. This EVM features a parallel interface to communicate to any host processor base system.

## 1.2 Power Requirements

The following sections describe the power requirements of this EVM.

### 1.2.1 Supply Voltage

The dc power supply requirement for the digital section of this EVM is typically 5 V connected to the J11-2 or via J6-2 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J11-1 and J6-1 terminal. The dc power supply requirement for the analog section ($V_{CC}$ and $V_{SS}$) of this EVM range from 15.75 V to -15.75 V maximum and connects through J10-4 and J12-1 or through J7-6 and J7-8 terminals and is referenced to analog ground through J10-2, J12-2 and J7-1 terminals.

A dc source of ±15 V supply is required to provide the rails for the external output op-amp provided for output signal conditioning or boost capacitive load drive and for other output modes of application. The 15 V supply connects through J10-1 or J7-2 terminal, and the –15 V supply connects through J10-3 or J7-4 terminals. The ±15 V supply is referenced to ground through J10-2 or J7-3 terminals. The supply source for $V_{CC}$ and $V_{SS}$ can also be used as the supply source for 15 V and -15 V respectively.

CAUTION

**To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.**

**Stresses above the maximum listed voltage ratings may cause permanent damage to the device.**

### 1.2.2 Reference Voltage

Although the DAC7741 has a built-in 10-V voltage reference, an external reference circuit is provided in the EVM board. The external reference circuit can be isolated if the internal reference voltage is selected.

The 10-V precision voltage reference is provided to supply the external voltage reference for the DAC through REF102, U3, via jumper W4 by shorting pins 1 and 2. An adjustable 100-kΩ potentiometer, R11, is installed in series with 20 kΩ, R10, to allow the user to adjust the reference voltage to its desired settings. TP1 and TP2 are also provided, as well as J4-20, to allow the user to connect other external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed 10-V dc.

The REF102 precision reference derives its power of ±15-V supply through J10 or J7 terminal. The (plus) 15 V connects through J10-1 or J7-2 terminals, while the (minus) -15 V connects through J10-3 or J7-4 terminals. They are both referenced to analog ground through J10-2 and J7-1.

The DAC7741 has a $\overline{\text{REFEN}}$ pin to enable the internal reference circuit or disable it and select an external reference source. The $\overline{\text{REFEN}}$ pin can be hardware driven through W2 jumper. Likewise, it can also be software driven through J2-11 terminal via W2 jumper by shorting pins 1 and 2. The $REF_{OUT}$ pin of the DAC7741 must be connected to the $REF_{IN}$ pin to use the internal voltage reference. This can be done through W3 jumper by shorting pins 1 and 2. Shorting pins 2 and 3 of W3 selects the external voltage reference source.

The on-chip reference buffer output is channeled out through $V_{REF}$ pin which is used to set up the DAC7741 output amplifier into one of three voltage output modes. $V_{REF}$ can also be used to drive other system components that require external voltage reference.

CAUTION

**When applying an external voltage reference through TP1 or J4-20, make sure that it does not exceed 10 V maximum. Otherwise, this can permanently damage the DAC7741, U11, device under test.**

## 1.3 EVM Basic Functions

The DAC7741 EVM is a functional evaluation platform to test certain functional characteristics of the DAC7741 digital-to-analog converter. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TMS320VC33™ DSP, or some sort of a waveform generator.

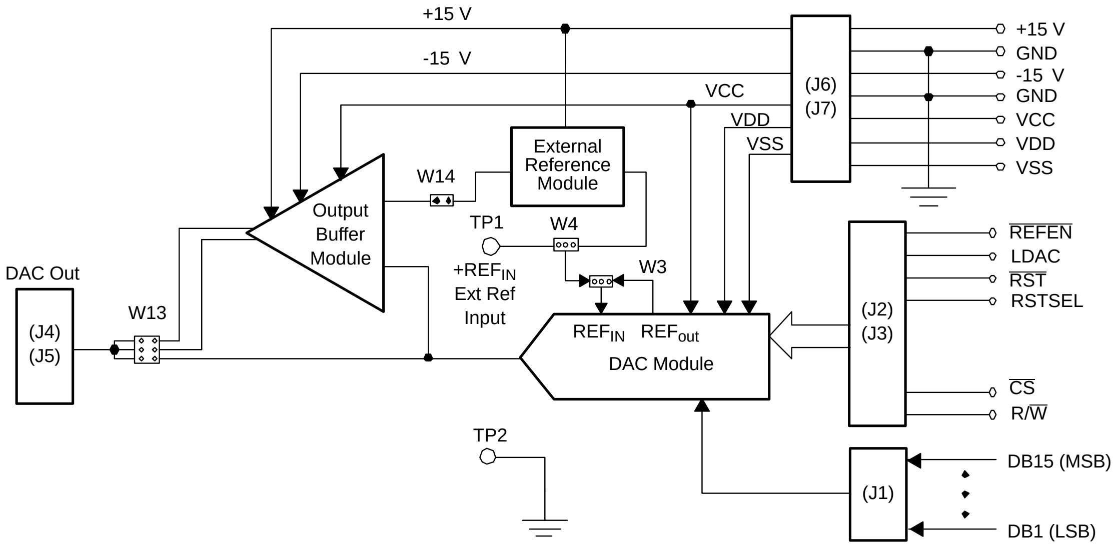
The headers, J1, J2 and J3 are provided to channel in the necessary control signals and data needed to interface a microprocessor/microcontroller, TI's DSP starter kit or waveform generator to the DAC7741 EVM, through a custom cable.

A specific adapter interface card is also available for most of TI's DSP starter kit (DSK) and the card model depend on the type of the DSP starter kit to be used. The user must specify the DSP used as an interface to acquire the right adapter interface card. Call or email TI for more information regarding the adapter interface card.

The output of the DAC can be monitored through two different access points which are as follows; a BNC connector (J5, if installed), and also a header through pin 2 of J4. The 6-pin header, W13, provides different options of the DAC output, but requires the output op-amp, U2, to be configured correctly first for the desired waveform characteristic. Shorting pins 1 and 2 of W13 allows the user to monitor the raw output of the DAC7741.

A block diagram of the EVM is shown below in the Figure 1-1.

*Figure 1-1. EVM Block Diagram*



Chapter 2

# Physical Description

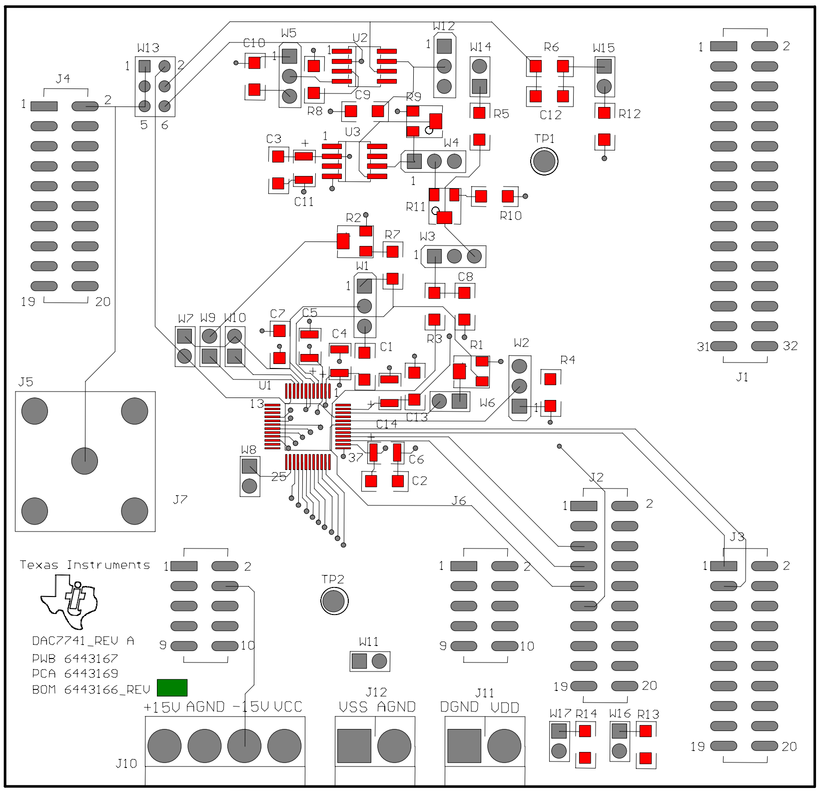
This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

**Topic** **Page**

## 2.1 PCB Layout

The EVM is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 99,06 mm (3.90 inch) × 104,14 mm (4.10 inch), and the board thickness is 1,57 mm (0.062 inch). Figures 2-1 through 2-6 show the individual artwork layers.

*Figure 2-1. Layer One (Top Silkscreen)*




DAC7741 REV A LAYER 1 SILKSCREEN TOP

*Figure 2-2. Layer Two (Ground Plane)*

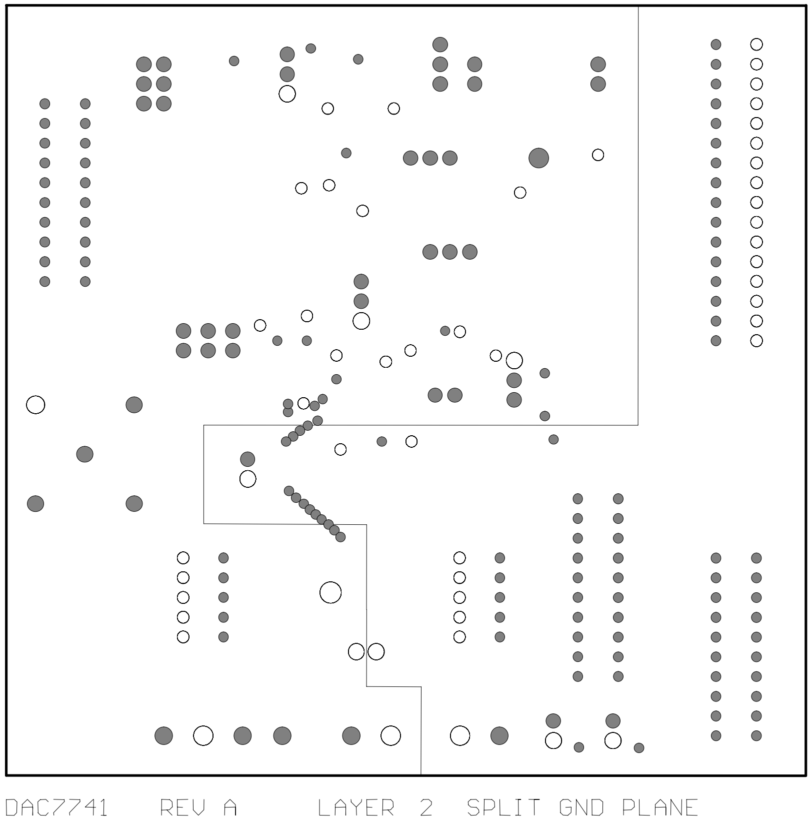


*Figure 2-3. Layer 3 (Power Plane)*

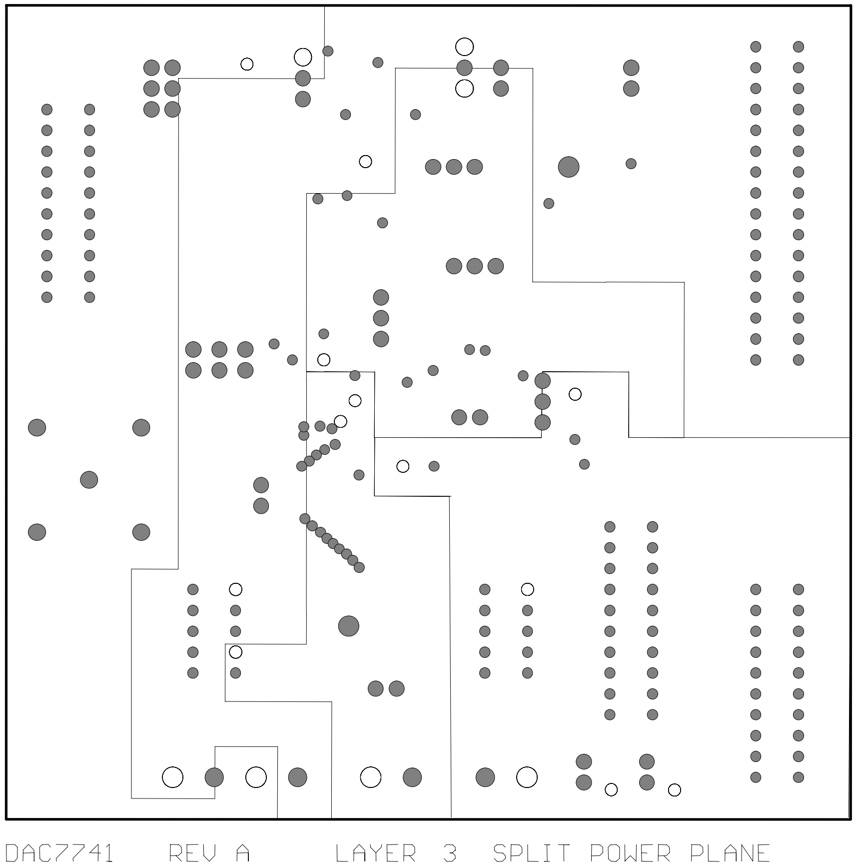


*Figure 2-4. Layer 4 (Bottom Plane)*

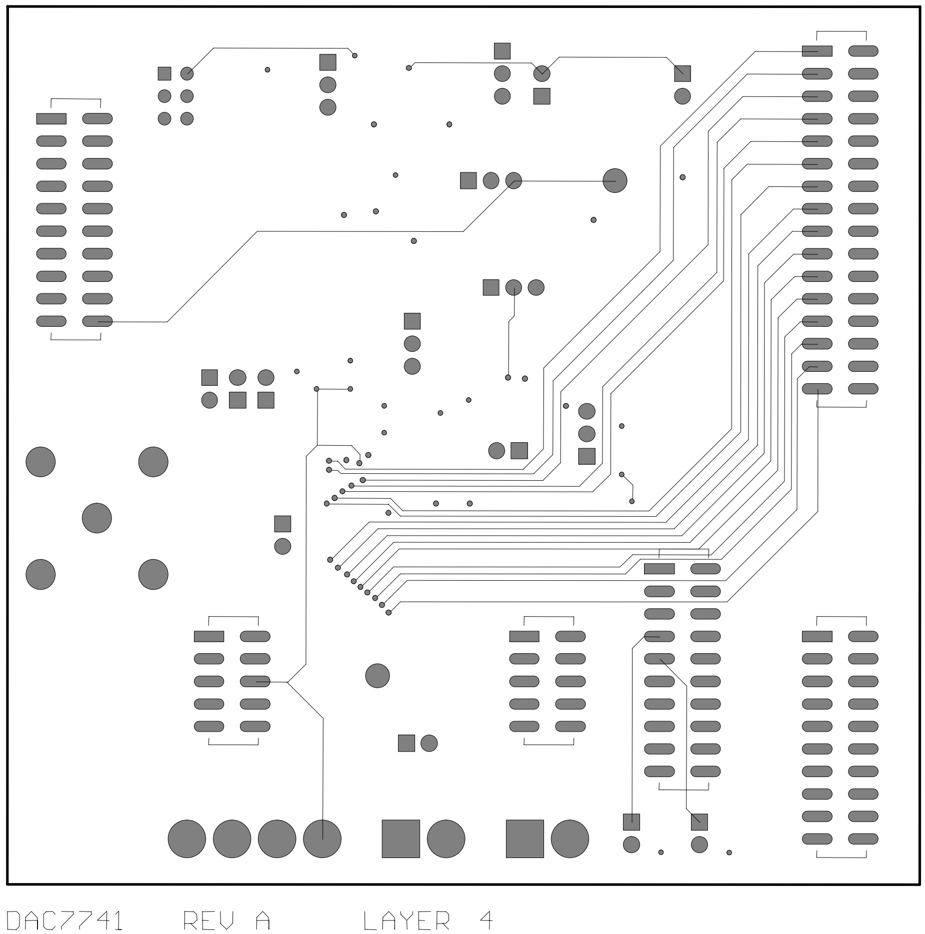
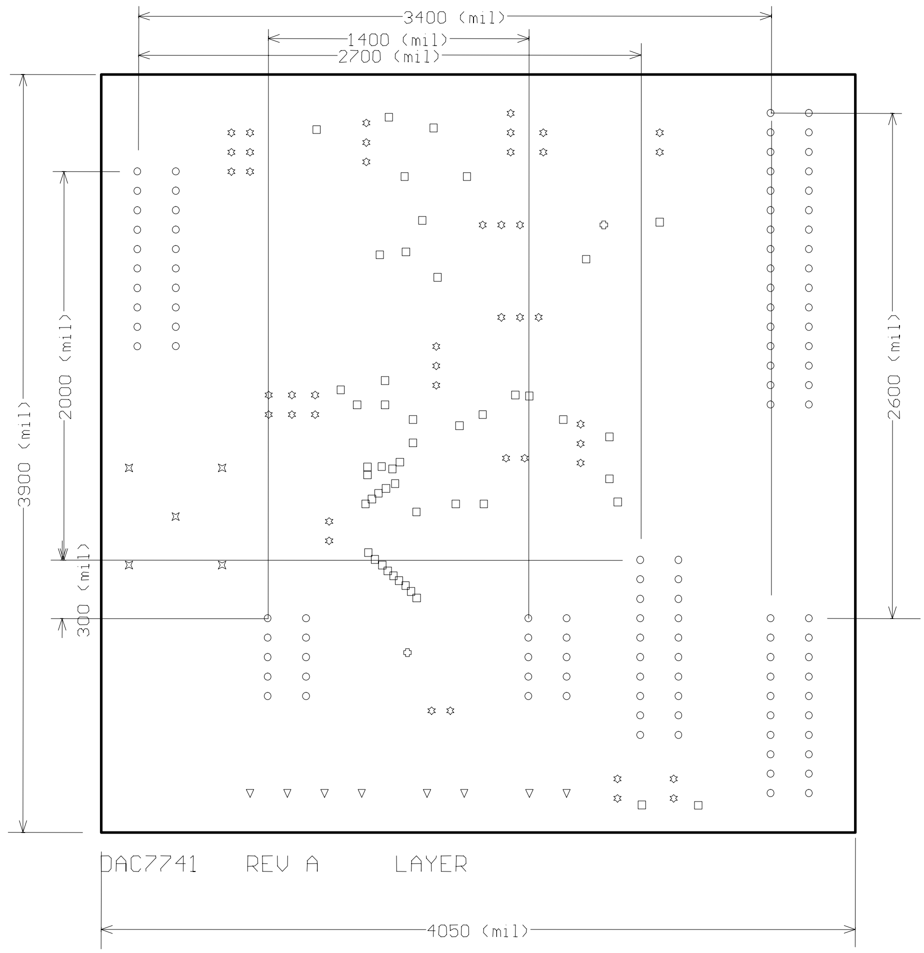


*Figure 2-5. Drill Drawing*



## 2.2 Bill of Materials

*Table 2-1. Parts List*

| Item # | Qty | Designator | Manufacturer | Part Number | Description |
|---|---|---|---|---|---|
| 1 | 1 | C8 | Panasonic | ECJ3VB1C105K | 1 μF, 1206 multilayer ceramic capacitor |
| 2 | 2 | C9 C10 | Panasonic | ECUV1H103KBM | 0.01 μF, 1206 multilayer ceramic capacitor |
| 3 | 5 | C1 C2 C3 C7 C13 | Panasonic | ECJ3VB1C104K | 0.1 μF, 1206 multilayer ceramic capacitor |
| 4 | 1 | C12 | Panasonic | ECUV1H102JCH | 1 nF, 1206 multilayer ceramic capacitor |
| 5 | 5 | C4 C5 C6 C11 C14 | Kemet | C1210C106K8PAC | 10 μF, 1210 multilayer ceramic X5R capacitor |
| 6 | 1 | R8 | Panasonic | ERJ-8GEY0R00V | 0 Ω, 1/4W 1206 chip resistor |
| 7 | 2 | R7 R10 | Panasonic | ERJ-8ENF2002V | 20 kΩ, 1/4W 1206 chip resistor |
| 8 | 6 | R4 R5 R6 R12 R13 R14 | Panasonic | ERJ-8ENF1002V | 10 kΩ, 1/4W 1206 chip resistor |
| 9 | 2 | R1 R2 | Bourns | 3214W-103E | 10 kΩ, BOURNS_32X4W Series 5T pot |
| 10 | 1 | R11 | Bourns | 3214W-104E | 100 kΩ, BOURNS_32X4W Series 5T pot |
| 11 | 1 | R3 | Panasonic | ERJ-8ENF1003V | 100 kΩ, 1/4W 1206 chip resistor |
| 12 | 2 | J6 J7 | Samtec | IPT1-105-01-S-D-VS | 5X2X0.1<br>10-pin 3A isolated power socket |
| 13 | 3 | J2 J3 J4 | Samtec | TSM-1 10-01-S-DV-M | 10X2X.1, 20-pin 0.025” sq SMT socket |
| 14 | 1 | J1 | Samtec | TSM-1 16-01-S-DV-M | 16X2X.1, 32-pin 0.025” sq SMT socket |
| 15 | 2 | J11 J12 | Lumberg | KRMZ2 | 2-pin Terminal screw connector |
| 16 | 1 | J5 (Not Installed) | AMP (TYCO) | 227699-2 | PCB Mounted BNC - Amphenol |
| 17 | 1 | J10 | Lumberg | KRMZ4 | 4-pin Terminal screw connector |
| 18 | 1 | U1 | Texas Instruments | DAC7741 | 16-bit, 48-LQFP DAC |
| 19 | 1 | U2 | Texas Instruments | OPA627AU | 8-SOP(D) Precision op amp |
| 20 | 1 | U3 | Texas Instruments | REF102AU | 10 V, 8-SOP(D) Precision voltage reference |
| 21 | 2 | TP1 TP2 | Cambion | 180-7337-02-05 | Turret terminal test point |
| 22 | 1 | W13 | Samtec | TSW-103-07-L-D | 3X2X 0.1 6-Pin IDC header |
| 23 | 3 | P2 P3 P4 (see Note) | Samtec | SSW-1 10-22-S-D-VS-P | 20-pin 0.025” sq SMT terminal strips |
| 24 | 1 | P1 (see Note) | Samtec | SSW-1 16-22-S-D-VS-P | 32-pin 0.025” sq SMT Terminal Strips |
| 25 | 2 | P6 P7 (see Note) | Samtec | IPS1-105-01-S-D-VS | 3A Isolated power header |
| 26 | 10 | W6 W7 W8 W9 W10 W11 W14 W15 W16 W17 | Samtec | TSW-102-07-L-S | 2 Position jumper_ 0.1” spacing |
| 27 | 6 | W1 W2 W3 W4 W5 W12 | Samtec | TSW-103-07-L-S | 3 Position Jumper_ 0.1” spacing |
| 28 | 1 | R9 | Bourns | 3214W-203E | 20 kΩ, BOURNS_32X4W Series 5T pot |

**Note:** P1, P2, P3, P4, P8, & P9 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC Board opposite the J designated counterpart. Example, J1 is installed on the topside while P1 is installed in the bottom side opposite of J1.

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**Chapter 3**

# EVM Operation

This chapter covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

Refer to the DAC7741 data sheet, SBAS248, for information about its parallel interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

**Topic** **Page**

## 3.1 Factory Default Setting

The EVM board is set to its default configuration from factory as described on the table below to operate in bipolar ±10V mode of operation using the internal reference.

*Table 3-1. Factory Default Jumper Setting*

| Reference | Jumper Position | Function |
|---|---|---|
| W1 | OPEN | $V_{REF}$ output pin is floated and not used for offset adjustment. |
| W2 | 2-3 | $\overline{REFEN}$ pin is tied to AGND to enable 10 V internal reference. |
| W3 | 1-2 | $REF_{OUT}$ pin is strapped to $REF_{IN}$ to provide 10 V internal voltage reference. |
| W4 | OPEN | Onboard external reference through U3 is disconnected. |
| W5 | 1-2 | Negative supply rail of U2 op-amp is supplied with -15 V. |
| W6 | OPEN | REFADJ pin is floated. |
| W7 | CLOSE | RFB2 pin is strapped to $V_{OUT}$ pin for DAC output feedback. |
| W8 | CLOSE | TEST pin is tied to DGND. |
| W9 | OPEN | SJ pin is floated. |
| W10 | OPEN | RFB1 is floated. |
| W11 | CLOSE | AGND and DGND are tied together to a common point. |
| W12 | 1-2 | Positive supply rail of U2 op-amp is supplied with 15 V. |
| W13 | 3-4 | Buffered output of DAC is channeled through to J5 and J4-2. |
| W14 | OPEN | External reference is disconnected from the negative input of U2 to configure U2 for unity gain. |
| W15 | OPEN | Configure U2 op-amp for unity gain. |
| W16 | OPEN | RSTSEL pin is tied high to set DAC reset value to midscale. |
| W17 | OPEN | $\overline{RST}$ pin is tied high by default. |

## 3.2 Host Processor Operation

The host processor basically drives the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 and J3 header connectors for the control signals, and J1 header connector for the data input. The output can be monitored through the J5 BNC connector (if installed) or J4 header connector. An interface adapter card is also available for specific DSP starter kits as mentioned in Chapter 1 of this manual.

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. This is set to a unity gain configuration by default. Regardless, the raw output of the DAC can be probed through W13 pin 2 so that it can be compared with the output of U2 if necessary. The output terminals J5 and J4 are provided to monitor the desired output of the DAC by shorting the respective pins of W13.

The following sections describe the different configurations of the output amplifier, U2.

### 3.2.1 Unity Gain Output

The buffered output configuration is used to prevent loading the DAC7741 and should closely match the raw output of the DAC with maybe some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R7 and C11 and replacing them with the desired values. You can also simply get rid of R7 and C11 altogether and just solder a zero-Ω resistor in replacement of R7, if desired.

Table 3-2 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

*Table 3-2. Unity Gain Output Jumper Settings*

| Reference | Jumper Setting | | Function |
|---|---|---|---|
| | Unipolar | Bipolar | |
| W5 | 2-3 | 1-2 | Supplies the voltage for the negative rail of op-amp. |
| W12 | 2-3 | 1-2 | Supplies the voltage for the positive rail of op-amp. |
| W13 | 3-4 | 3-4 | DAC output is channeled to the output terminals. |
| W14 | Open | Open | exREFin is disconnected from the negative input of op-amp. |
| W15 | Open | Open | Disconnect negative input of op-amp from GND |

### 3.2.2 Output Gain of Two

This configuration allows the DAC output with a gain of two, but is limited to the effective rails of the operational amplifier. When the DAC7741 is configured to operate in bipolar mode, the DAC output must be within the range of 12 $V_{P-P}$ or less. Anywhere above the range of 12 $V_{P-P}$ would clip the output of the op-amp. Likewise, when operating the DAC in unipolar mode, the DAC output must not exceed 6 $V_{P-P}$.

Table 3-3 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

*Table 3-3. Gain of Two Output Jumper Settings*

| Reference | Jumper Setting | Function |
|---|---|---|
| W5 | 1-2 (Bipolar)<br>2-3 (Unipolar) | Negative rail of the op-amp tied to -15 V for bipolar operation or AGND for unipolar operation. |
| W12 | 1-2 | Positive rail supply of the op-amp tied to 15 V |
| W13 | 3-4 | Amplified output of DAC is channeled to the output terminals |
| W14 | Open | Disconnect exREFin from negative input of op-amp |
| W15 | Close | Configures op-amp for a 2× gain output |

### 3.2.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all op-amps under certain conditions may become unstable depending on the op-amp configuration, gain, and load value. These are just few factors that can affect op-amps stability performance and should be considered when implementing.

In unity gain, the OPA627 op-amp, U2, performs very well with very large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and by adding a load resistor would even improve the capacitive load drive capability.

Table 3-4 shows the jumper setting configuration for a capacitive load drive.

*Table 3-4. Capacitive Load Drive Output Jumper Settings*

| Reference | Jumper Setting | Function |
|---|---|---|
| W5 | 1-2 (Bipolar)<br>2-3 (Unipolar) | Negative rail of the op-amp tied to -15 V for bipolar operation or AGND for unipolar operation. |
| W12 | 1-2 | Positive rail supply of the op-amp tied to 15 V |
| W13 | 5-6 | Capacitive load drive output of DAC is channeled to the output terminals |
| W14 | Open | Disconnect exREFin from negative input of op-amp |
| W15 | Open | Disconnect R12 (see note) |

**Note:** If there is a need to incrementally adjust the capacitive load output, replace R12 with a capacitor with the desired capacitance value and CLOSE W15.

## 3.3 Jumper Setting

The figures in Table 3-5 will show the function of each jumper on the EVM.

*Table 3-5. Jumper Setting Function*

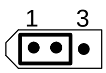
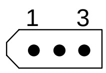
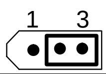
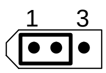
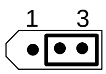
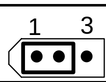
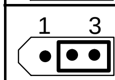
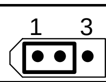
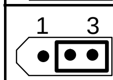
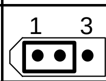
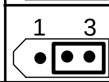
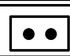
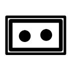
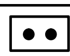
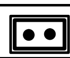
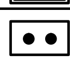
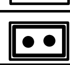
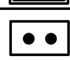
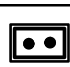
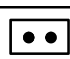
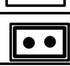
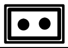
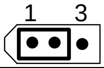
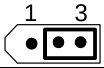
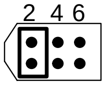
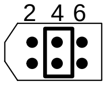
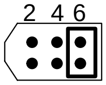
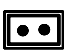
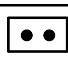
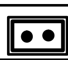
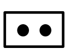
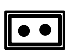
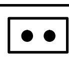
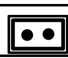
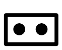
| Reference | Jumper Setting | Function |
|---|---|---|
| W1 |  | $R_{OFFSET}$ is strapped to $V_{REF}$ to set $V_{SJ}$ (summing junction) to $V_{REF}/2$. Refer to the data sheet for offset adjustment. |
| |  | $R_{OFFSET}$ is not connected to set $V_{SJ}$ (summing junction) to $V_{REF}/3$. Refer to the data sheet for offset adjustment. |
| |  | $R_{OFFSET}$ is strapped to AGND to set $V_{SJ}$ (summing junction) to $V_{REF}/6$. Refer to the data sheet for osset adjustment. |
| W2 |  | Disables the internal reference voltage. |
| |  | Enables the internal reference voltage of +10V. |
| W3 |  | $REF_{IN}$ is strapped to $REF_{OUT}$ to allow the internal 10 V to supply the DAC reference voltage. |
| |  | $REF_{IN}$ is strapped to exREFin to allow either the onboard adjustable reference or user supplied reference to supply the DAC reference voltage. |
| W4 |  | Routes the onboard 10 V reference through the adjustable pot to W3 and W14. |
| |  | Routes the user supplied reference from TP1 or J4-20 through the adjustable pot to W3 and W14. |
| W5 |  | Negative supply rail of op-amp is powered by -15 V. |
| |  | Negative supply rail of op-amp is tied to AGND. |
| W6 |  | REFADJ pin is not connected. |
| |  | REFADJ pin is connected to R1 pot for gain adjustment input when internal reference is used. |
| W7 |  | RFB2 pin is not connected to the $V_{OUT}$ pin. |
| |  | RFB2 pin is strapped to the $V_{OUT}$ pin for feedback. |
| W8 |  | TEST pin not connected to DGND. |
| |  | TEST pin connected to DGND (default mode). |
| W9 |  | SJ (summing junction) pin of the DAC output amplifier is not connected. |
| |  | SJ (summing junction) pin of the DAC output amplifier is connected to R2 pot to allow small amount of current for offset adjustment. |
| W10 |  | RFB1 pin is not connected. |
| |  | RFB1 pin is strapped to RFB2 pin for DAC $V_{OUT}$ feedback. |

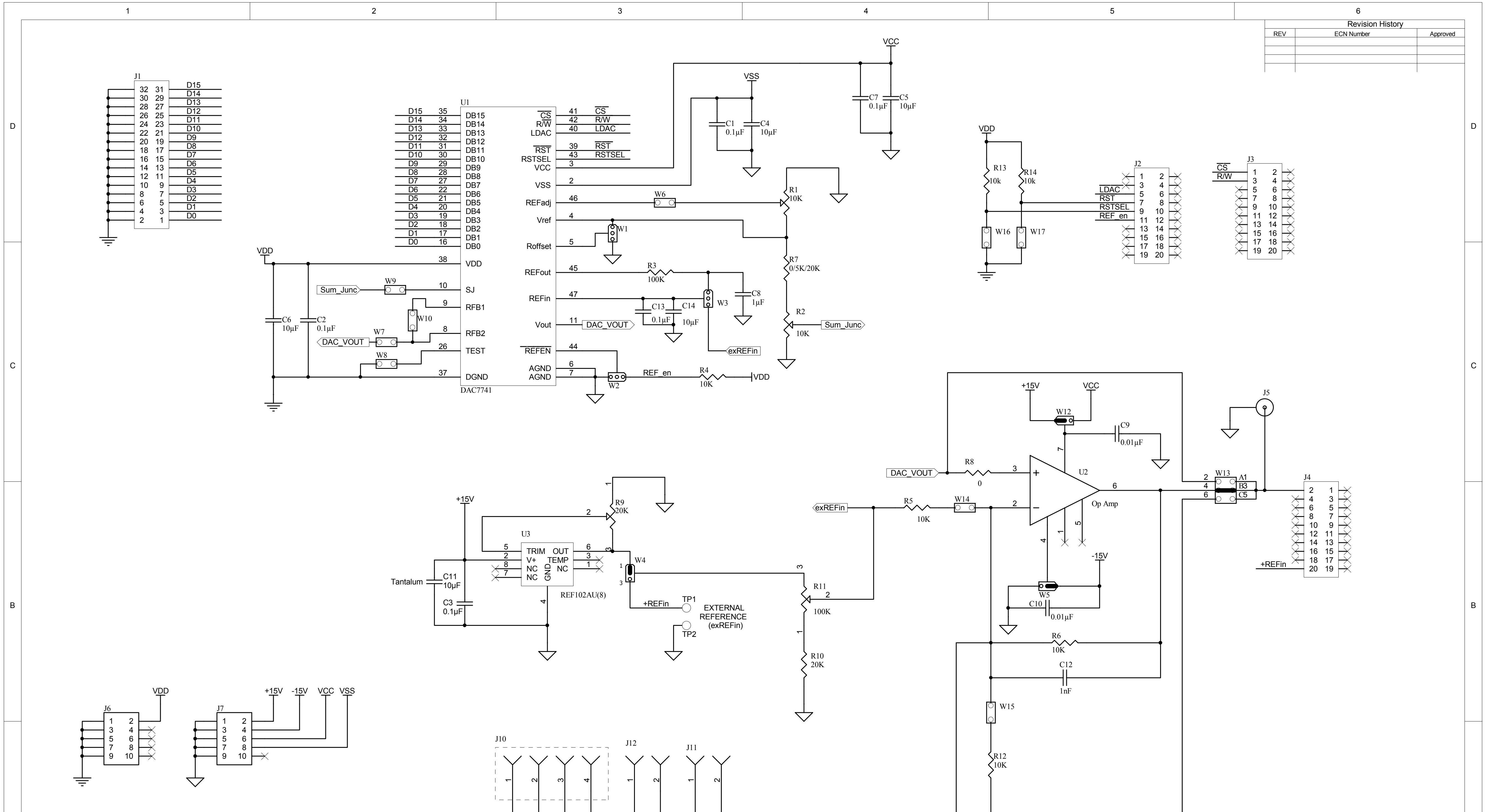
*Table 3-5. Jumper Setting Function (Continued)*

| Reference | Jumper Setting | Function |
|---|---|---|
| W11 |  | Disconnects AGND from DGND. |
| |  | Connects AGND and DGND together. |
| W12 | 1 3  | Positive supply rail of op-amp is powered by +15V. |
| | 1 3  | Positive supply rail of op-amp is powered by $V_{CC}$. |
| W13 | 2 4 6  1 3 5 | Routes the raw output of the DAC7741 to J4-2 and J5 output terminals. |
| | 2 4 6  1 3 5 | Routes the output of U2 to J4-2 and J5 output terminals. Used for unipolar and bipolar modes of operation. |
| | 2 4 6  1 3 5 | Routes the output of U2 to J4-2 and J5 output terminals. Used for capacitive load driving. |
| W14 |  | Disconnects exREFin from the negative input terminal of U2. |
| |  | Allows exREFin to be routed to the negative input terminal of U2 used for experimentation purposes only. |
| W15 |  | Disconnect the negative terminal of U2 to AGND and disable 2x gain. |
| |  | Configures U2 for a 2× gain output. |
| W16 |  | RSTSEL pin is pulled high and configures the DAC to midscale when POR or reset is initiated. |
| |  | RSTSEL pin is pulled low and configures the DAC to minscale when POR or reset is initiated. |
| W17 |  | $\overline{\text{RST}}$ pin is pulled high and configures the DAC not to reset (default state). |
| |  | $\overline{\text{RST}}$ pin is pulled low and holds the DAC to reset state. |

**Legend:**  Indicates the corresponding pins that are shorted or closed.

## 3.4 Schematic

A schematic of the DAC7741 is found on the following page.




TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

| | | | |
|---|---|---|---|
| Title: | DAC7741 | | |
| Engineer: J. PARGUIAN | DOCUMENTCONTROL # 6443168 | REV: A | |
| Drawn By: | | | |
| FILE: DAC7741.Sch | DATE: 27-Sep-2002 | SIZE: | SHEET: 1 OF: 1 |